In re Patent Application of
**LIBRIZZI**
Serial No. **NOT YET ASSIGNED**
Filed: **HEREWITH**
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**In the Claims:**

Claims 1-7 (canceled).

8. (New) A control circuit for a PWM regulator that receives a square wave signal having a duty cycle and provides a regulated direct current (DC) signal at an output thereof, the PWM regulator comprising a switching device for modulating the duty cycle of the square wave signal, the control circuit comprising:

detector means for detecting trailing edges of the square wave signal and providing a reset signal based thereon;

ramp signal generator means connected to said detector means for generating a ramp signal based upon leading edges of the square wave signal, and for resetting the ramp signal based upon the reset signal;

first comparator means connected to the output of the PMW regulator for comparing the regulated DC signal with a reference signal and providing an error signal based thereon;

second comparator means for comparing the ramp signal with the error signal and providing a PMW signal based thereon; and

driver means for driving the switching device of the PWM regulator circuit, said driver means receiving the PWM signal and providing a driving signal for driving the switching device based thereon to control a conduction interval thereof, the driving signal having a duty cycle less than or equal to the duty cycle of the square wave signal and

also having trailing edges substantially coinciding with the trailing edges of the square wave signal.

9. (New) The control circuit of Claim 8 wherein said first comparator means comprises an error amplifier.

10. (New) The control circuit of Claim 8 wherein said second comparator means comprises an error amplifier.

11. (New) The control circuit of Claim 8 wherein said second comparator means provides the PWM signal when the ramp signal is greater than the error signal.

12. (New) The control circuit of Claim 8 wherein said driver means comprises a bistable circuit having a first input for receiving the PWM signal and a second input for receiving the reset signal.

13. (New) The control circuit of Claim 12 further comprising a delay element connected to the second input of said bistable circuit for delaying the reset signal.

14. (New) The control circuit of Claim 12 wherein said bistable circuit comprises a set-reset (S-R) flip-flop; and wherein the first input of said S-R flip-flop comprises a set input, and the second input of said S-R flip-flop comprises a reset input.

15. (New) A control circuit for a PWM regulator that receives a square wave signal having a duty cycle and modulates the duty cycle to provide a regulated direct current (DC) signal at an output thereof, the control circuit comprising:

a detector for detecting trailing edges of the square wave signal and providing a reset signal based thereon;

a ramp signal generator connected to said detector for generating a ramp signal based upon leading edges of the square wave signal, and for resetting the ramp signal based upon the reset signal;

a first comparator connected to the output of the PMW regulator for comparing the regulated DC signal with a reference signal and providing an error signal based thereon;

a second comparator for comparing the ramp signal with the error signal and providing a PMW signal based thereon; and

a driver for controlling modulation of the square wave signal duty cycle by the PWM regulator, said driver receiving the PWM signal and providing a driving signal based thereon, the driving signal having a duty cycle less than or equal to the duty cycle of the square wave signal and also having trailing edges substantially coinciding with the trailing edges of the square wave signal.

16. (New) The control circuit of Claim 15 wherein said first comparator comprises an error amplifier.

17. (New) The control circuit of Claim 15 wherein said second comparator comprises an error amplifier.

18. (New) The control circuit of Claim 15 wherein said second comparator provides the PWM signal when the ramp signal is greater than the error signal.

19. (New) The control circuit of Claim 15 wherein said driver comprises a bistable circuit having a first input for receiving the PWM signal and a second input for receiving the reset signal.

20. (New) The control circuit of Claim 19 further comprising a delay element connected to the second input of said bistable circuit for delaying the reset signal.

21. (New) The control circuit of Claim 19 wherein said bistable circuit comprises a set-reset (S-R) flip-flop; and wherein the first input of said S-R flip-flop comprises a set input, and the second input of said S-R flip-flop comprises a reset input.

22. (New) A PWM regulator for receiving a square wave signal having a duty cycle and providing a regulated direct current (DC) signal at an output thereof and comprising:

a switching device for modulating the duty cycle of the square wave signal; and

a control circuit for controlling said switching device and comprising

a detector for detecting trailing edges of the square wave signal and providing a reset signal based thereon,

a ramp signal generator connected to said detector for generating a ramp signal based upon leading edges of the square wave signal, and for resetting the ramp signal based upon the reset signal,

a first comparator connected to the output of the PMW regulator for comparing the regulated DC signal with a reference signal and providing an error signal based thereon,

a second comparator for comparing the ramp signal with the error signal and providing a PMW signal based thereon, and

a driver for receiving the PWM signal and providing a driving signal for driving said switching device based thereon to control a conduction interval thereof, the driving signal having a duty cycle less than or equal to the duty cycle of the square wave signal and also having trailing edges coinciding with the trailing edges of the square wave signal.

23. (New) The PWM regulator of Claim 22 wherein said first comparator comprises an error amplifier.

24. (New) The PWM regulator of Claim 22 wherein said second comparator comprises an error amplifier.

25. (New) The PWM regulator of Claim 22 wherein said second comparator provides the PWM signal when the ramp signal is greater than the error signal.

26. (New) The PWM regulator of Claim 22 wherein said driver comprises a bistable circuit having a first input for receiving the PWM signal and a second input for receiving the reset signal.

27. (New) The PWM regulator of Claim 26 wherein said control circuit further comprises a delay element connected to the second input of said bistable circuit for delaying the reset signal.

28. (New) The PWM regulator of Claim 26 wherein said bistable circuit comprises a set-reset (S-R) flip-flop; and wherein the first input of said S-R flip-flop comprises a set input, and the second input of said S-R flip-flop comprises a reset input.

29. (New) A method for modulating a duty cycle of a square wave signal to provide a regulated direct current (DC) signal using a switching circuit, the method comprising:

detecting trailing edges of the square wave signal and providing a reset signal based thereon;

generating a ramp signal based upon leading edges of the square wave signal and resetting the ramp signal based upon the reset signal;

comparing the regulated DC signal with a reference signal and providing an error signal based thereon;

comparing the ramp signal with the error signal and providing a PMW signal based thereon; and

controlling modulation of the square wave signal duty cycle by generating a driving signal for the switching circuit based upon the PWM signal, the driving signal having a duty cycle less than or equal to the duty cycle of the square wave signal and also having trailing edges substantially coinciding with the trailing edges of the square wave signal.

30. (New) The method of Claim 29 wherein providing the PWM signal comprises providing the PWM signal when the ramp signal is greater than the error signal.